Amendments To The Specification

Please replace paragraph [0033] in the Specification page 10, lines 3-4 with the following amended paragraph:

[0033] Subsequently, a silicon nitride layer 112 also to be referred to as a fourth inter-insulation layer is formed on the third inter-insulation layer 111.

Please replace paragraph [0034] in the Specification page 10, lines 5-11 with the following amended paragraph:

[0034] As shown in FIGS. 2d, 3d and 4d, a photosensitive layer pattern 113 is formed on the silicon nitride layer (a.k.a., the fourth inter-insulation layer) 112, in which bit line contact areas are defined on the photosensitive layer pattern 113. Subsequently, the silicon nitride layer (a.k.a., the fourth inter-insulation layer) 112 is etched to form a silicon nitride layer pattern (also to be referred to as a fourth inter-insulation layer pattern) 112a using the photosensitive layer pattern 113 as a mask as shown in FIG. 4D.

Please replace paragraph [0035] in the Specification page 10, lines 12-20 with the following amended paragraph:

[0035] As shown in FIGS. 2e, 3e and 4e, the photosensitive layer pattern is removed, and then the third and second inter-insulation layers 111 and 110 are etched to form bit line contacts 114 using the silicon nitride layer pattern

(a.k.a., a fourth inter-insulation layer pattern) 112a as a mask. Here, the bit line contacts 114 are applied by a self-aligned contact mode, so that, during the process of etching the bit line contacts, each bit line contact is formed only on the inside of each bit line defined in a Damascene process, but not on the outside of each bit line.

Please replace paragraph [0038] in the Specification page 11, lines 9-14 with the following amended paragraph:

[0038] Even if not shown in the drawings, a ~~fourth~~ fifth inter-insulation layer is formed on the resultant structure. The ~~fourth~~ fifth inter-insulation layer is alternatively etched to form storage node contacts. The storage node contacts are formed with insulation spacers, so that a short between the bit lines and the storage node contacts is prevented.

Please replace paragraph [0039] in the Specification page 15, lines 15-24 with the following amended paragraph:

[0039] In the present invention, the bit line contacts are formed in a self-aligned contact mode. As a result, as shown in FIG. 2f, the outer portions of the bit lines are not etched by the silicon nitride layer pattern (a.k.a. the fourth inter-insulation layer pattern) 112a, so that the bit line contacts 114 can be broadly formed in a direction in which the bit lines are to be formed.

That is, even though the bit line contacts 114 have a sufficiently large size, they are not formed on the outer portions of the bit lines. Thus, it is easy to fabricate the photosensitive layer pattern for forming the bit line contacts.